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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,058	03/02/2004	Yoshinori Wakimoto	118755	9834

25944 7590 03/27/2006

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,058	WAKIMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *2,4,6,8,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/790,058 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. The drawings are objected to because in Fig. 6 the input lines into the cascaded CAMs are not labeled. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. The information disclosure statement filed July 14, 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the document contains only the odd numbered pages (i.e. all the even numbered pages are missing). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. **As per claims 1 and 13**, the claims recite the limitation "the assignment" in lines 3-4 of each claim. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claims to read "an assignment."

7. **Also per claims 1 and 13**, the claims recite the limitation "the configuration" in line 5 of each claim. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claims to read "a configuration."

8. **Also per claims 1 and 13**, the claims recite the limitation "the logical bank" in lines 6 of each claim. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claims to read "a logical bank."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa et al. (Patent Abstracts of Japan, "Associative Memory," Publication

No. 2001-236790, published August 31, 2001) in view of Pereira et al. (U.S. Patent 6,493,793).

11. **As per claim 1**, Yoshizawa discloses a CAM device comprising:

a CAM array including a plurality of physical banks (paragraph 0011, lines 1-3; Fig. 1, element 12); *It should be noted that "associative memory array" is analogous to "CAM array."*

a logical bank-physical bank converter for setting the assignment between logical banks and physical banks, and for outputting a control signal to set the configuration of a physical bank assigned to the logical bank, depending on a logical bank signal indicating a logical bank to be searched (paragraph 0012, lines 1-4; paragraph 0022, lines 1-4; Fig. 1, element 14); *It should be noted that "logic and physical signal transformation circuit" is analogous to "logical bank-physical bank converter", "logic bank" is analogous to "logical bank", and "CONFIG <2:0>" is analogous to "control signal to set the configuration of a physical bank assigned to the logical bank."*

a priority circuit for outputting search results in accordance with predetermined priority (paragraph 0015, lines 1-4; Fig. 1, element 16). *It should be noted that "priority network" is analogous to "priority circuit", "HHA <14:0>" and "HEA <14:0>" are analogous to "search results."*

Yoshizawa does not expressly disclose a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and a search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device.

Pereira discloses a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and a search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device (col. 4, lines 48-51; col. 4, line 63 – col. 5, line 1; col. 5, lines 59-60; col. 6, lines 18-25; Fig. 1, element 100; Fig. 2, elements 204 and 205). *It should be noted that "cascade logic circuit" is analogous to "cascade circuit", "match flag logic" is analogous to "priority circuit", "/MFO" is analogous to "search results", "high-priority" is analogous to "high-order" and "low-priority" is analogous to "low-order."*

Yoshizawa and Pereira are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Pereira's cascade logic circuit with Yoshizawa's CAM array, logic and physical signal transformation circuit, and priority circuit.

The motivation for doing so would have been to gain the benefit of cascading a number of memory devices in a manner that achieves a balance between the number of match flag input pins and the time required to generate the system match flag (Pereira, col. 2, lines 43-45).

Therefore, it would have been obvious to combine Yoshizawa and Pereira for the benefit of obtaining the invention as specified in claim 1.

12. **As per claim 3**, Yoshizawa discloses when searching is performed, the logical bank-physical bank converter outputs, to each physical bank assigned to the logical

bank to be searched, a control signal for dynamically setting the configuration of the physical bank (paragraph 0022, lines 1-4).

13. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Pereira as applied to claim 1 above, and in further view of Lyon (U.S. Patent 6,493,812).

14. **As per claims 5 and 7**, Yoshizawa/Pereira discloses all the limitations of claims 5 and 7 except the logical bank-physical bank converter is capable of assigning one physical bank to two or more different logical banks.

Lyon discloses the logical bank-physical bank converter is capable of assigning one physical bank to two or more different logical banks (col. 2, lines 7-11). *It should be noted that "virtual" is analogous to "logical." It should also be noted that setting an assignment between virtual banks to physical banks the real procedure that is taking place is an assignment setting between the virtual and physical addresses of the banks.*

Yoshizawa/Pereira and Lyon are analogous art because they are from the same field of endeavor, that being addressing memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lyon's virtual address aliasing technique within Yoshizawa/Pereira's logic and physical signal transformation circuit.

The motivation for doing so would have been to increase memory performance by allowing cache data to be retained for multiple users and also access the cache data through different virtual addresses as the users change (Lyon, col. 7, lines 62-65).

Therefore, it would have been obvious to combine Yoshizawa/Pereira and Lyon for the benefit of obtaining the invention as specified in claims 5 and 7.

15. **Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Pereira as applied to claim 1 above, and in further view of Lyon as applied to claims 5 and 7 above, and in even further of Khanna et al. (U.S. Patent 6,393,514).**

16. **As per claims 9 and 11**, Yoshizawa/Pereira/Lyon discloses all of the limitations of claims 9 and 11 except said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI.

Khanna discloses said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7, element 64). *It should be noted that "match" is analogous to "hit." It should also be noted that the incorporated reference, Khanna (U.S. Patent 6,175,513), discloses an OR gate that inputs various multiple match flags and outputs an overall multiple match flag.*

Yoshizawa/Pereira/Lyon and Khanna are analogous art because they are from the same field of endeavor, that being content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Khanna's multiple match flag logic and full flag logic within Yoshizawa/Pereira/Lyon's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between write instructions which causes valid data to be written to the last available CAM row and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine Yoshizawa/Pereira/Lyon and Khanna for the benefit of obtaining the invention as specified in claims 9 and 11.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

17. **Claims 13-14** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

18. The primary reasons for allowance of **claims 13-14** in the instant application is the combination with the inclusion in these claims that "**while when the CAM device includes no physical bank assigned to the logical bank to be searched, a signal is output to indicate that there is no physical bank assigned to the logical bank.**" The prior art of record neither anticipates nor renders obvious the above recited combination.

19. **Claims 2, 4, 6, 8, 10, and 12** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. The primary reasons for allowance of **claims 2, 4, 6, 8, 10, and 12** in the instant application is the combination with the inclusion in these claims that "**wherein in searching, if the CAM device includes no physical bank assigned to a logical bank to be searched, the logical bank-physical bank converter outputs a signal to the cascade circuit to inform that there is no physical bank assigned to the logical bank; and in response to the signal, the cascade circuit outputs a signal indicating that the CAM device includes no hit entry.**" The prior art of record neither anticipates nor renders obvious the above recited combination.

21. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,374,326 discloses a multiple bank CAM architecture and method for performing multiple concurrent lookups with a CAM array.

2. U.S. Patent 6,512,684 discloses a CAM having cascaded sub-entry architecture.

3. U.S. Patent Application Publication 2003/0110329 discloses a circuit that sets a numerical value in a corresponding element when no virtual bank number is assigned to a physical bank.

4. Non-patent document Moors et al., "Cascading Content-Addressable Memories", June 1992, IEEE Micro, Volume 12, Issue 3, pp. 56-66 discloses cascaded CAMs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2185
March 17, 2006

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SUPERVISORY PATENT EXAMINER